FIG. 1(a) Prior Art

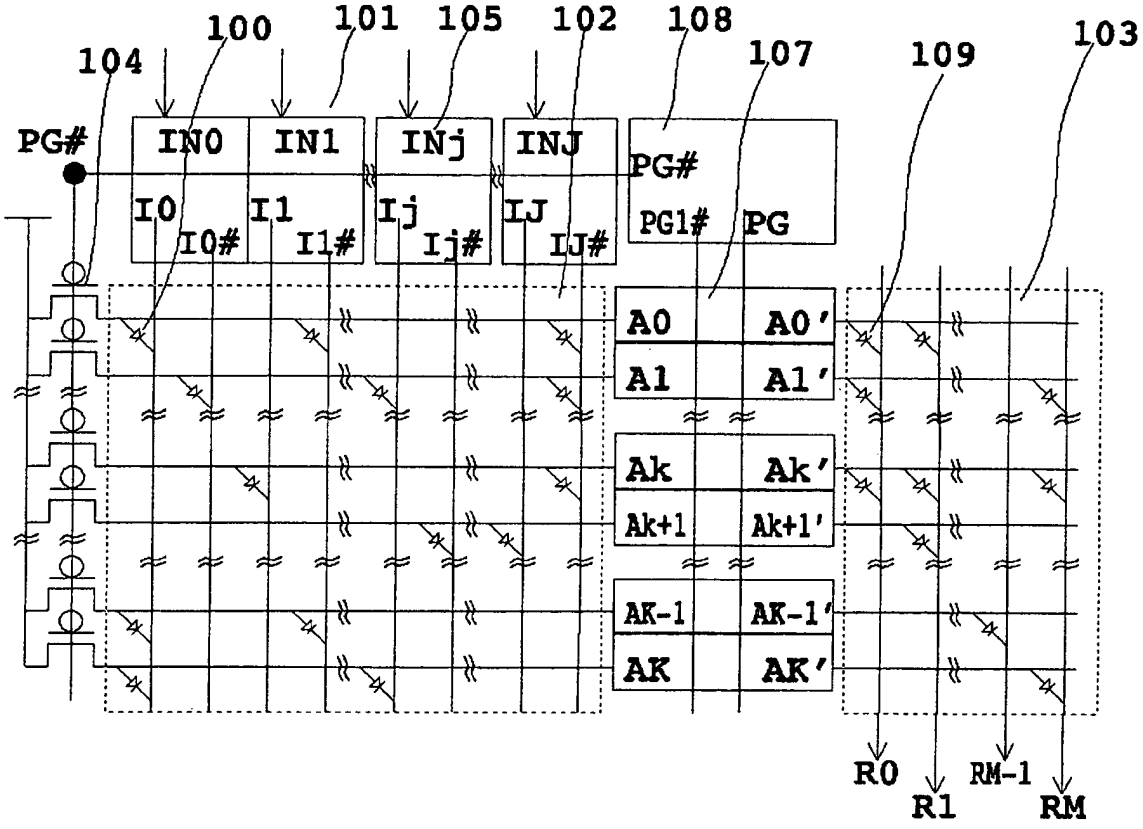

FIG. 1(b) Prior Art

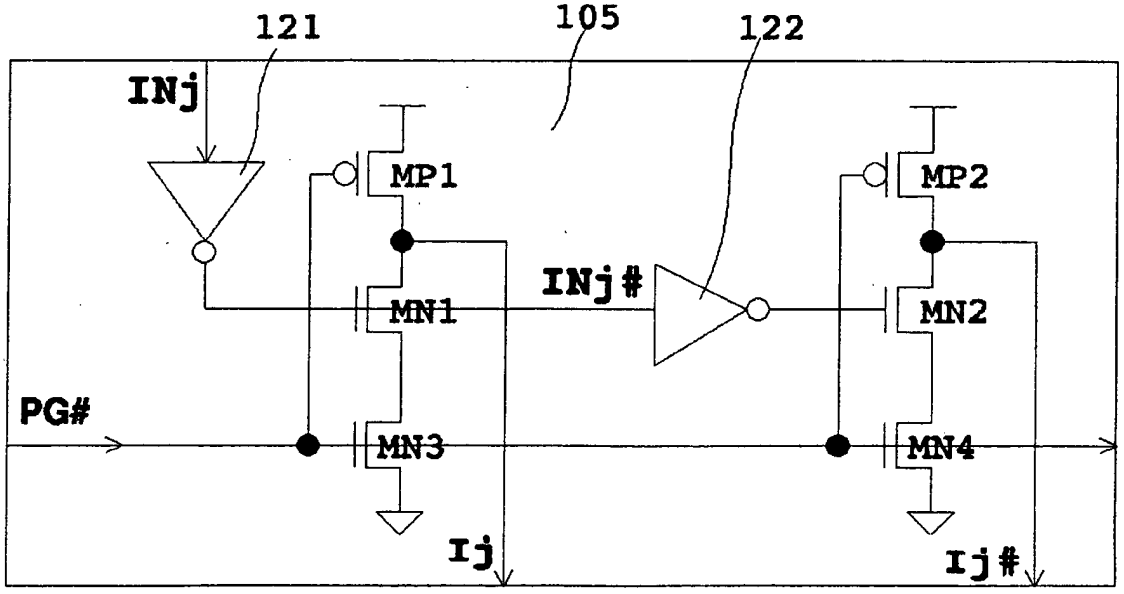

FIG. 1(c) Prior Art

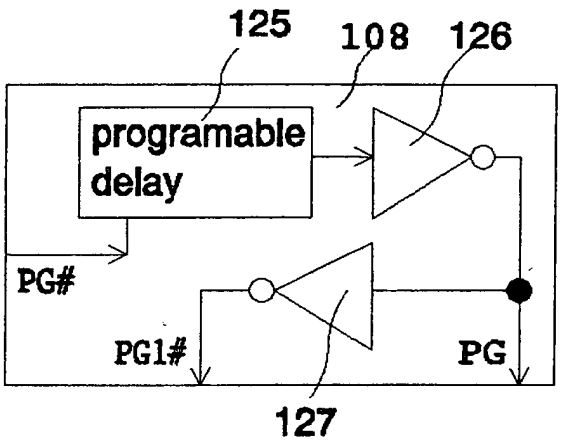

FIG. 1(d) Pri r Art

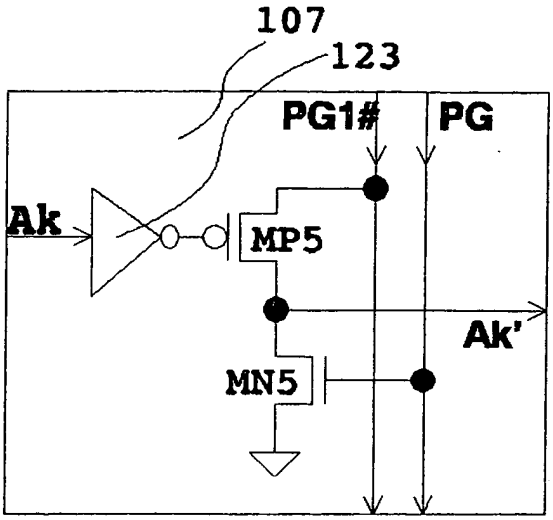

FIG. 1(e)Prior Art

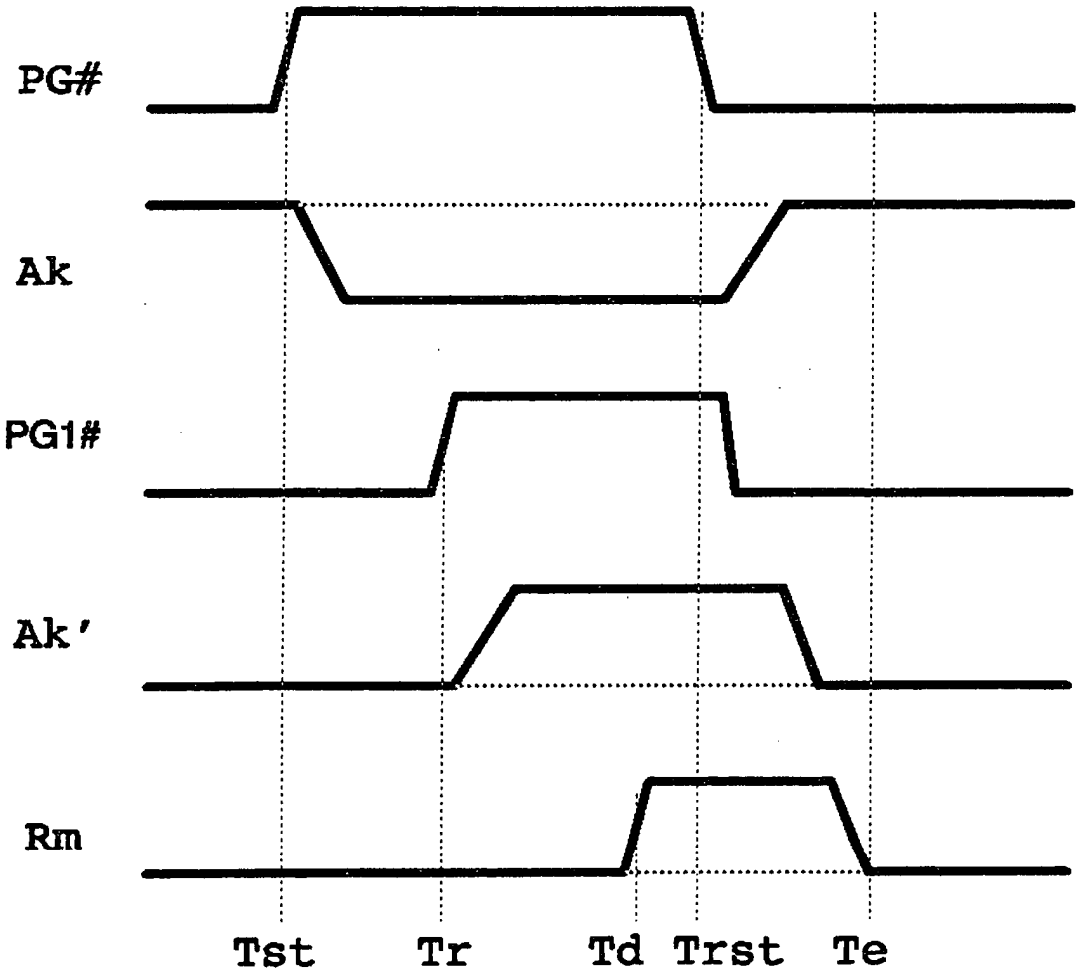

FIG. 1(f)

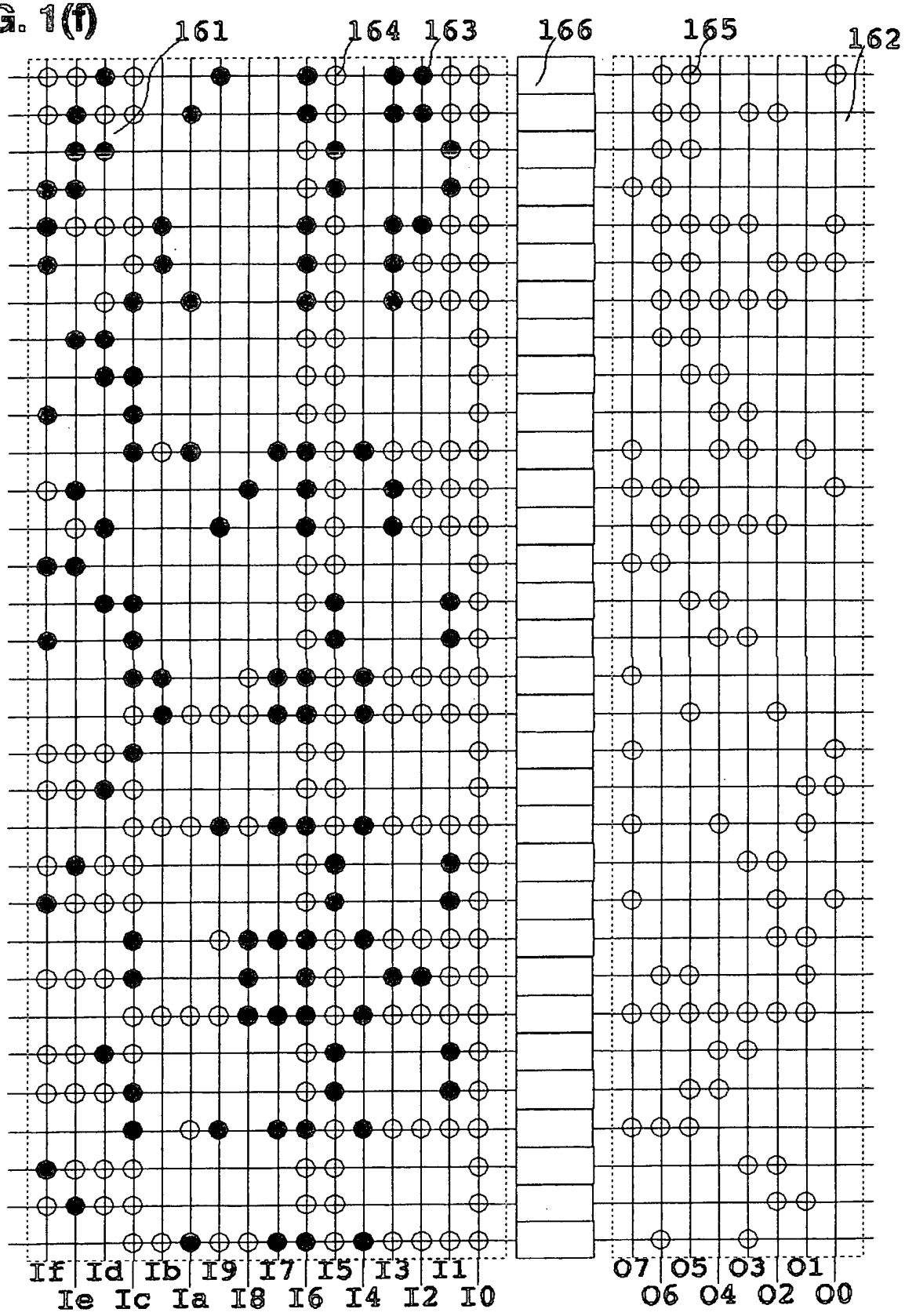
161
164
163
166
165
162
If
Id
Ib
I9
I7
I5
I3
I1
Ie
Ic
Ia
I8
I6
I4
I2
I0
O7
O5
O3
O1
O6
O4
O2
O0

FIG. 2(a)

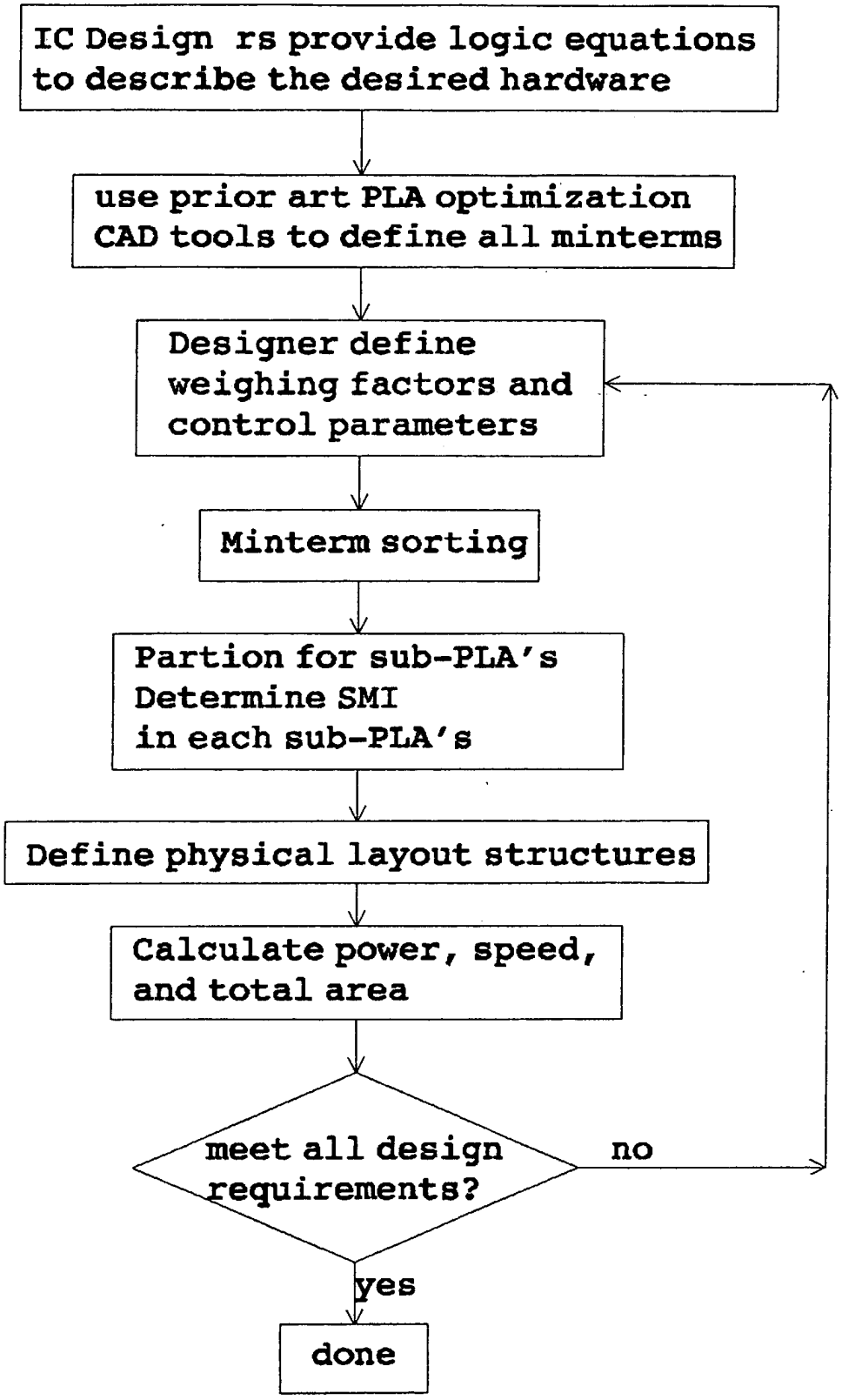
IC Design rs provide logic equations to describe the desired hardware
use prior art PLA optimization CAD tools to define all minterms
Designer define weighing factors and control parameters
Minterm sorting
Partion for sub-PLA's Determine SMI in each sub-PLA's
Define physical layout structures
Calculate power, speed, and total area
meet all design requirements?
no
yes
done

FIG. 2(b)

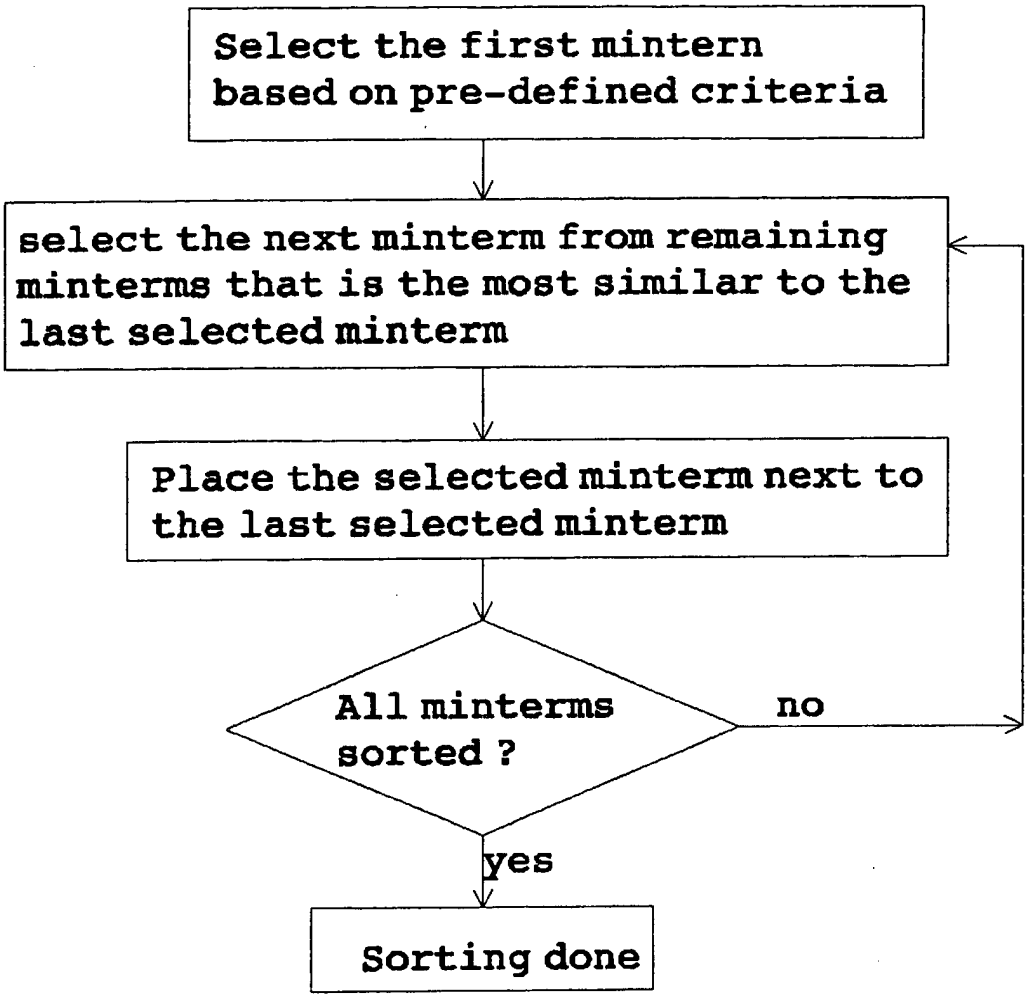
Select the first mintern based on pre-defined criteria
select the next minterm from remaining minterms that is the most similar to the last selected minterm
Place the selected minterm next to the last selected minterm
All minterms sorted ?
no
yes
Sorting done

FIG. 2(c)

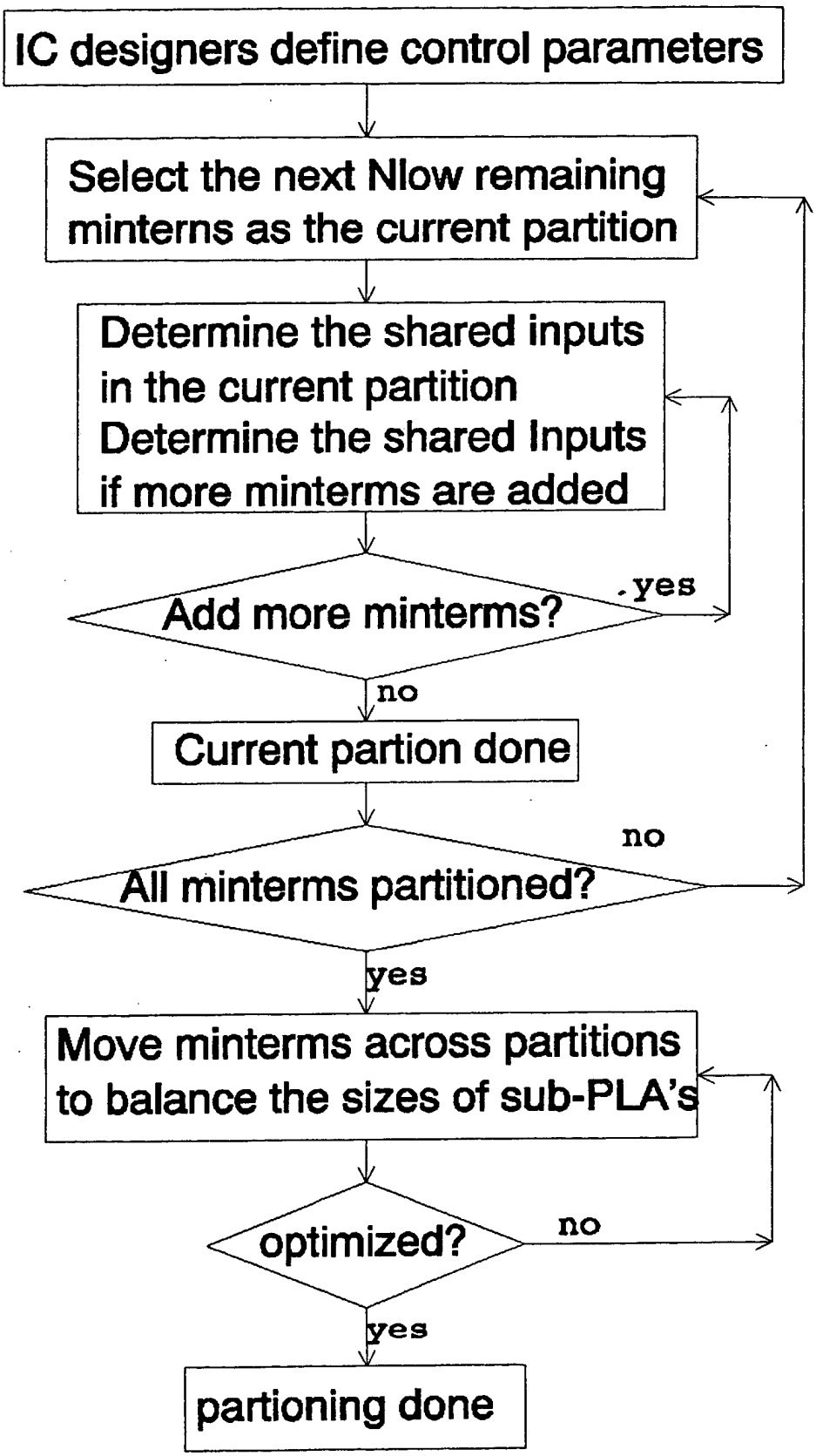
IC designers define control parameters
Select the next Nlow remaining minterms as the current partition
Determine the shared inputs in the current partition
Determine the shared Inputs if more minterms are added
Add more minterms?
yes
no
Current partion done
All minterms partitioned?
no
yes
Move minterms across partitions to balance the sizes of sub-PLA's
optimized?
no
yes
partioning done

FIG. 2(d)

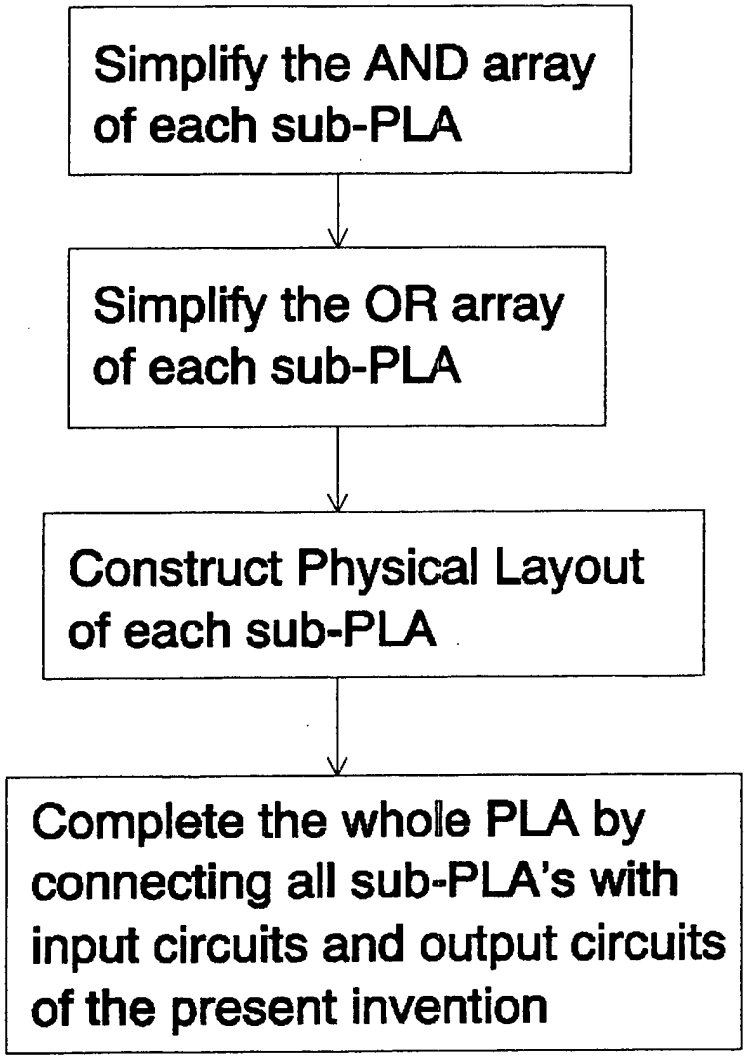
Simplify the AND array of each sub-PLA
Simplify the OR array of each sub-PLA
Construct Physical Layout of each sub-PLA
Complete the whole PLA by connecting all sub-PLA's with input circuits and output circuits of the present invention

FIG. 3(a)

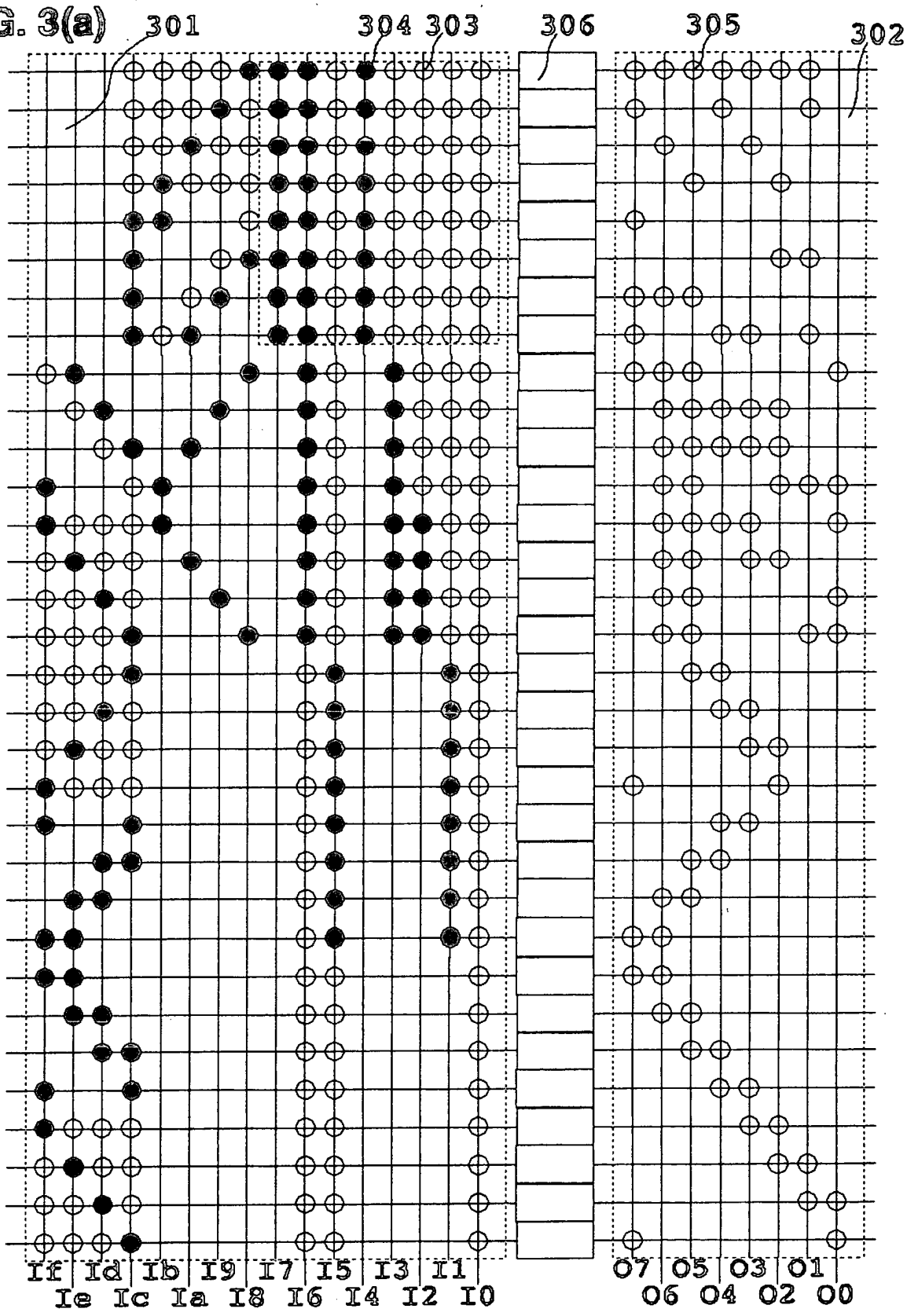
301
304
303
306
305
302
If
Id
Ib
I9
I7
I5
I3
I1
Ie
Ic
Ia
I8
I6
I4
I2
I0
O7
O5
O3
O1
O6
O4
O2
O0

FIG. 3(b)

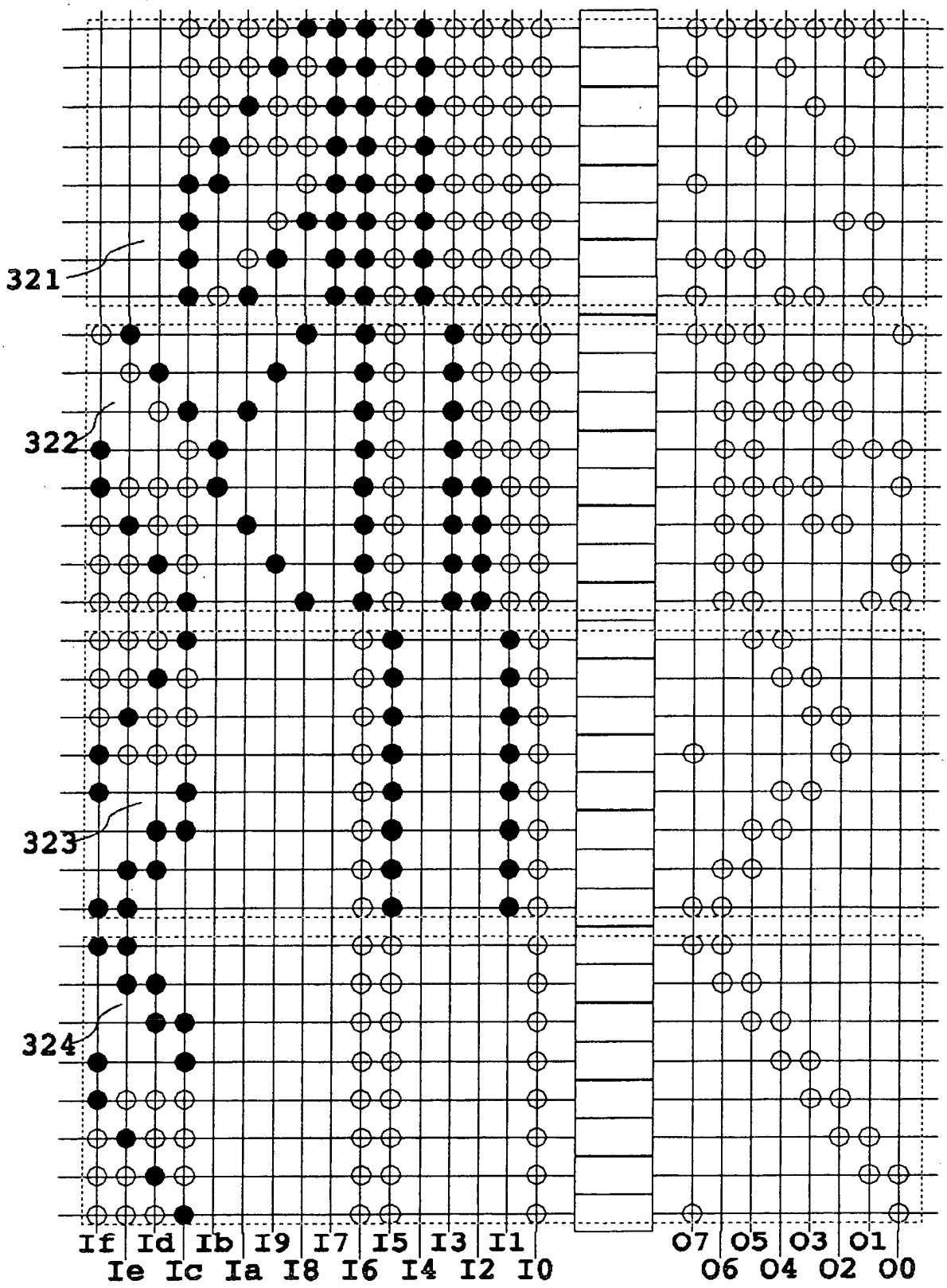
321
322
323
324
If Id Ib I9 I7 I5 I3 I1
Ie Ic Ia I8 I6 I4 I2 I0
O7 O5 O3 O1
O6 O4 O2 O0

FIG. 3(c)

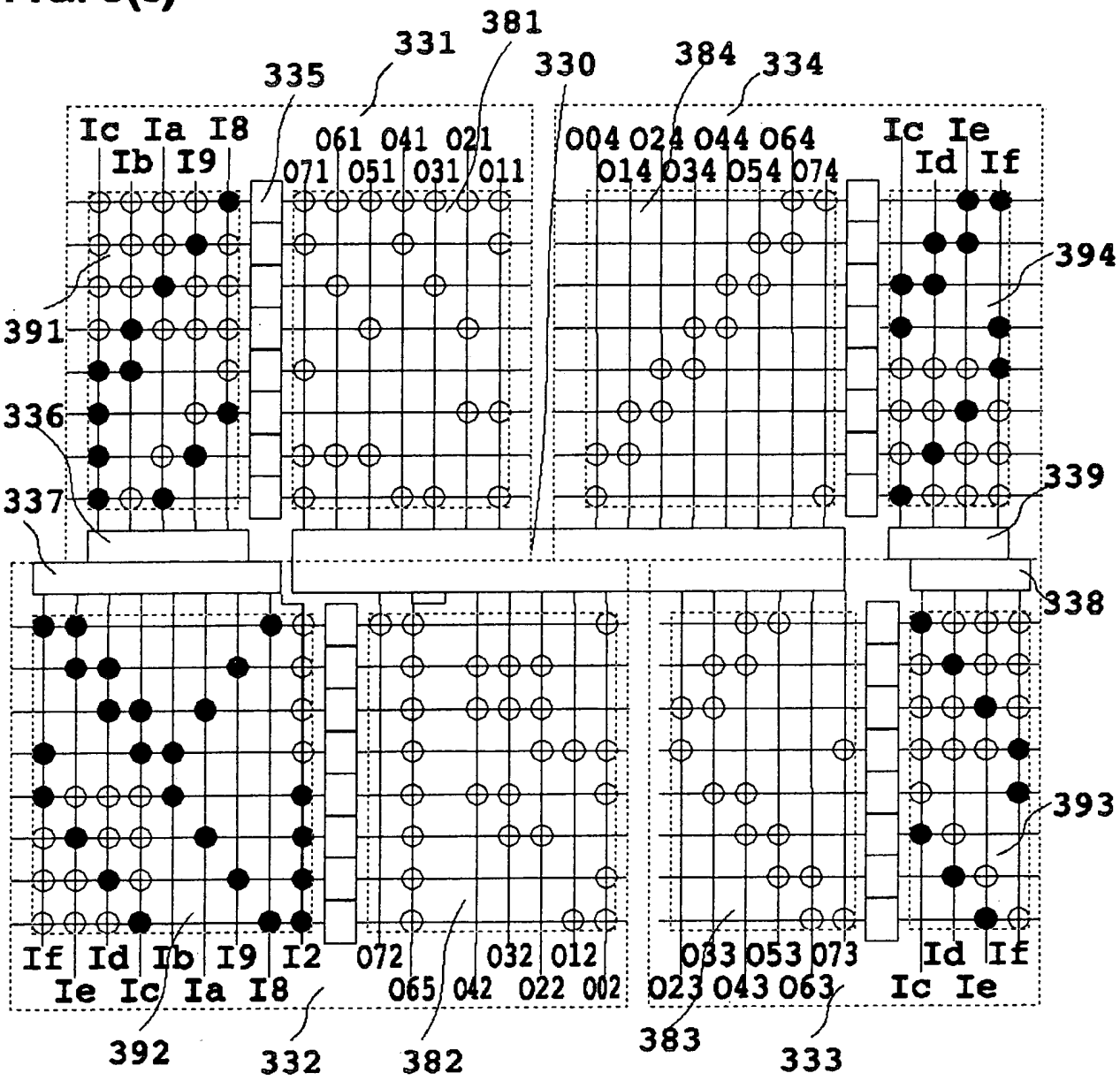
381
331
330
384
334
335
Ic Ia I8
Ib I9
061 041 021
071 051 031 011
004 024 044 064
014 034 054 074
Ic Ie
Id If
394
391
336
339
337
338
393
If Id Ib I9 I2
Ie Ic Ia I8
072
032 012
065 042 022 002
033 053 073
023 043 063
Id If
Ic Ie
392
332
382
383
333

FIG. 3(d)

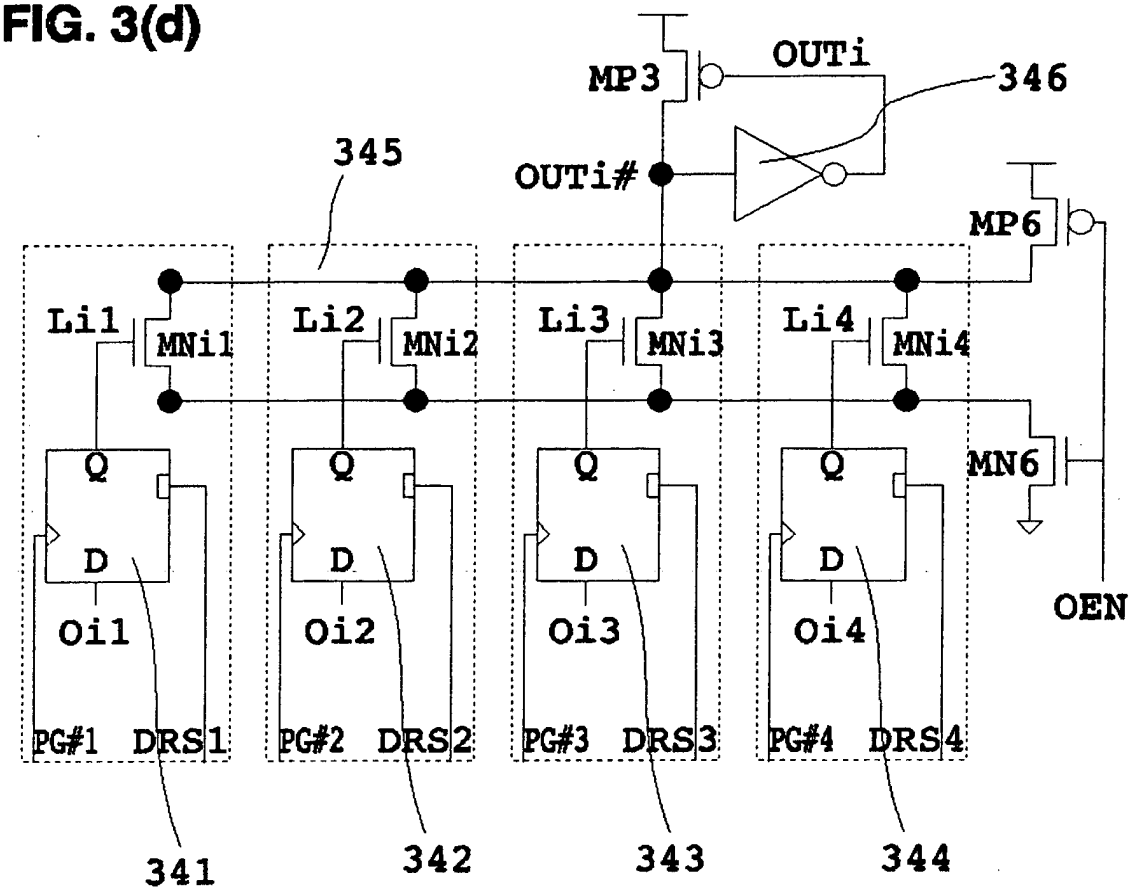
MP3
OUTi
346
345
OUTi#
MP6
Li1
MNi1
Li2
MNi2
Li3
MNi3
Li4
MNi4
Q
D
MN6
OEN
Oi1
Oi2
Oi3
Oi4
PG#1 DRS1
PG#2 DRS2
PG#3 DRS3
PG#4 DRS4
341
342
343
344

FIG. 3(e)

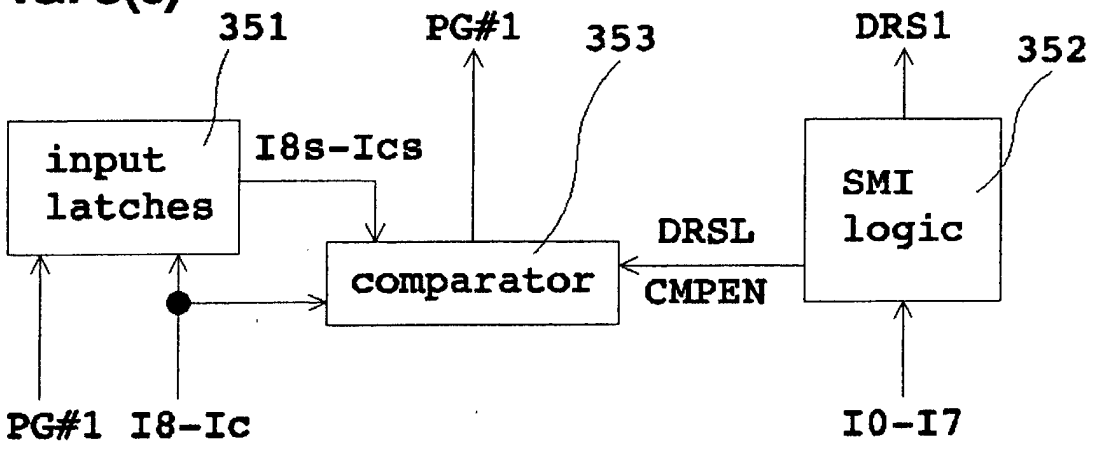
351
PG#1
353
DRS1
352
input latches
I8s-Ics
SMI logic
DRSL
comparator
CMPEN
PG#1 I8-Ic
I0-I7

FIG. 3(f)

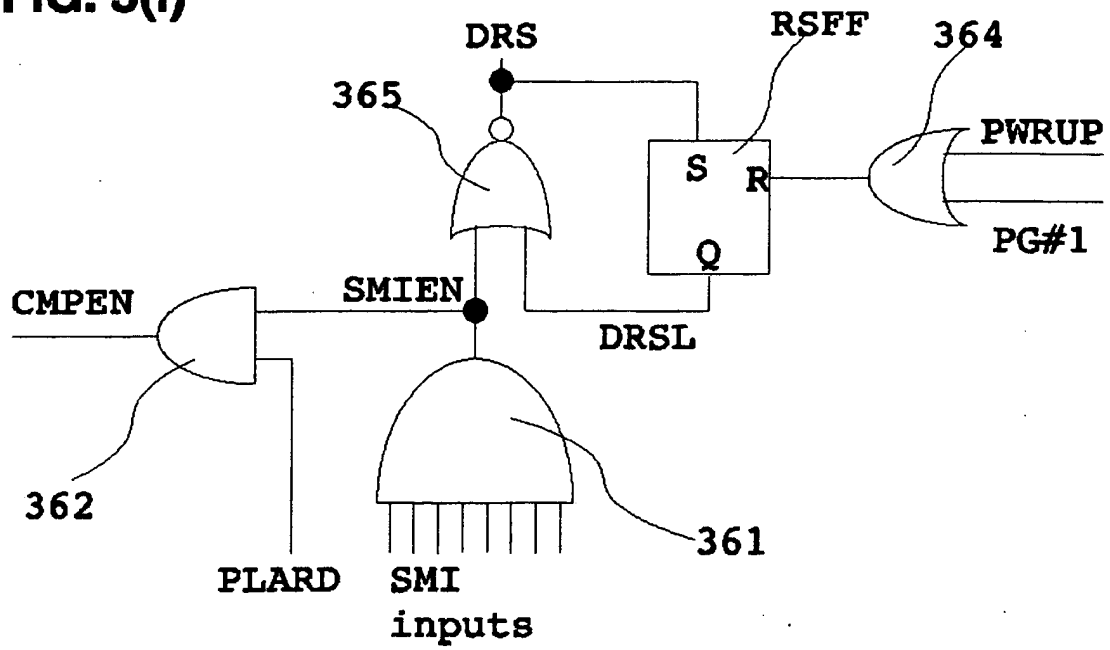
DRS
RSFF
364
365
PWRUP
S
R
Q
PG#1
CMPEN
SMIEN
DRSL
362
361
PLARD
SMI
inputs

FIG. 3(g)

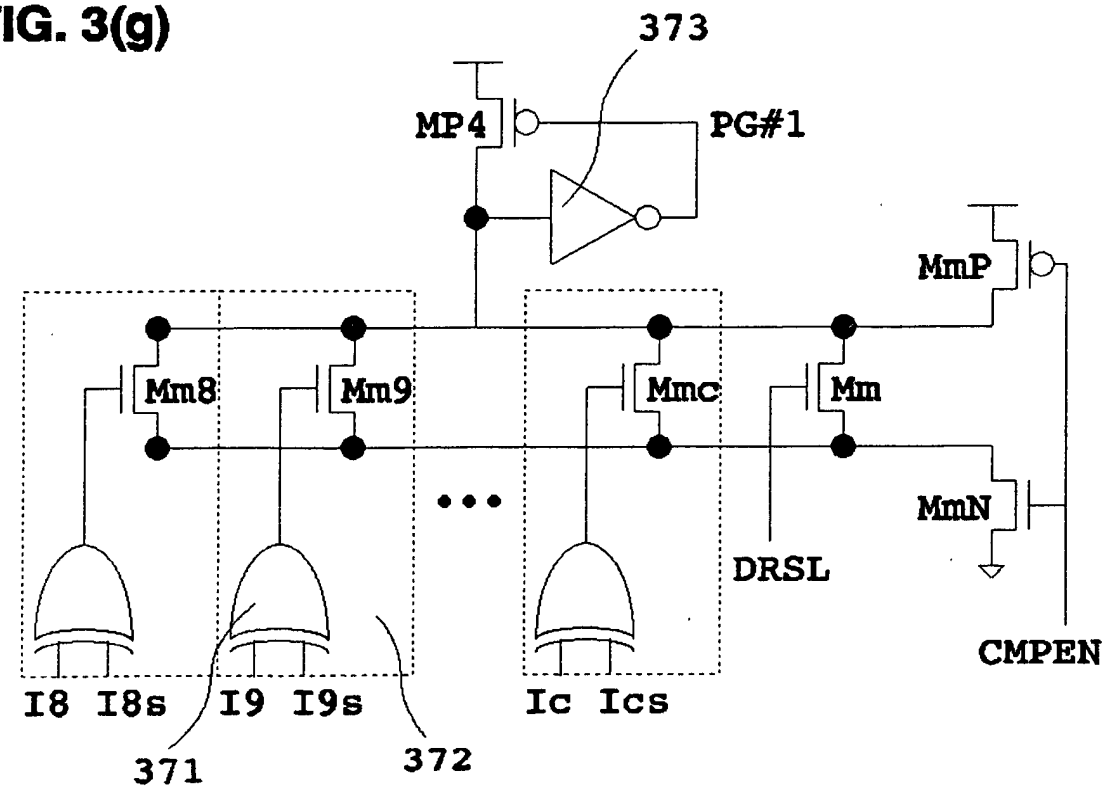
373
MP4
PG#1
MmP
Mm8
Mm9
Mmc
Mm
MmN
DRSL
CMPEN
I8
I8s
I9
I9s
Ic
Ics
371
372

FIG. 3(h)

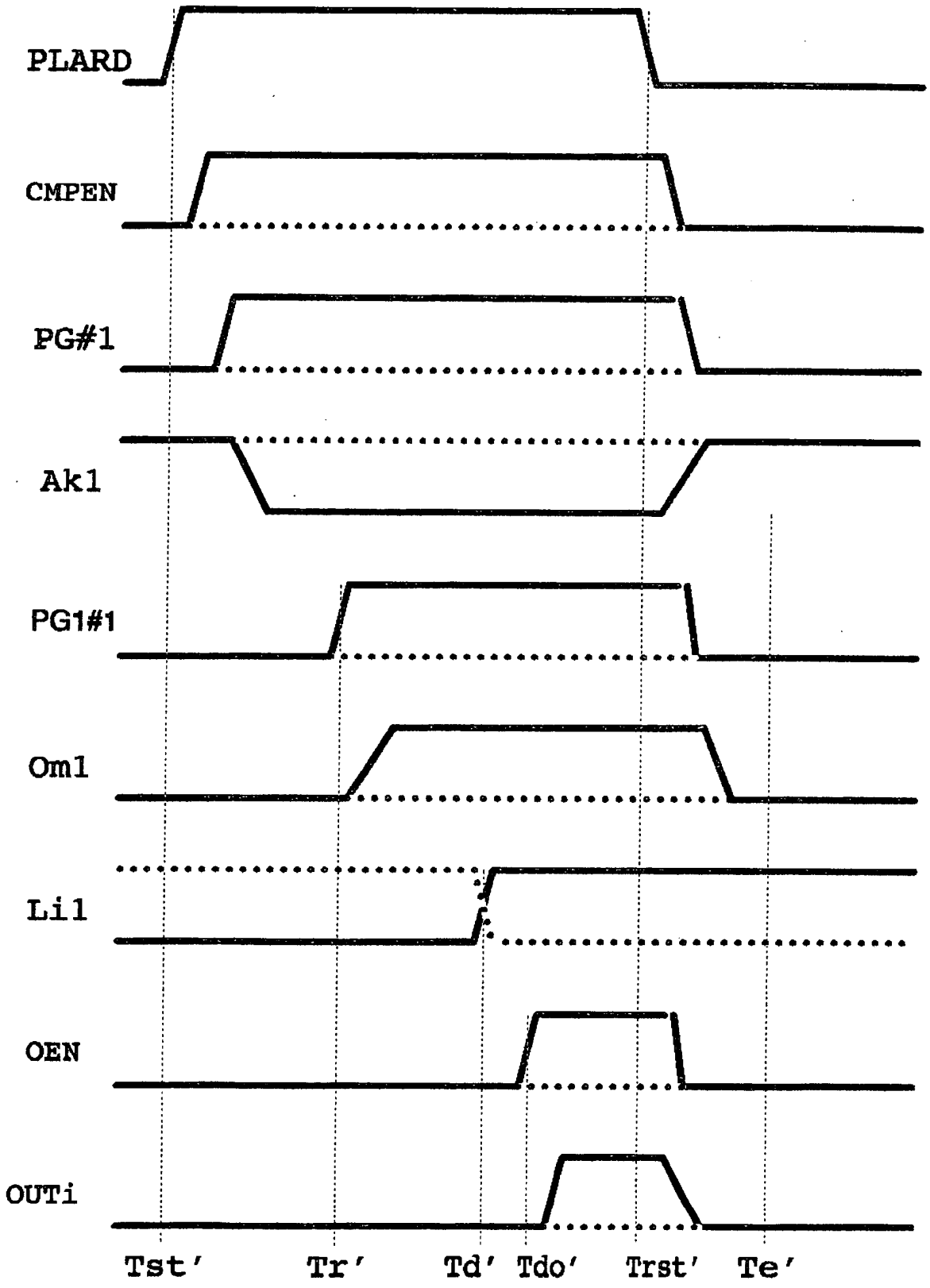

FIG. 4(a)

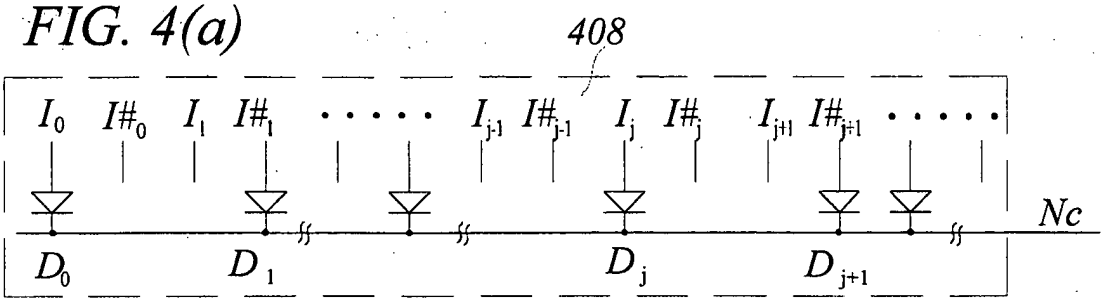

FIG. 4(b)

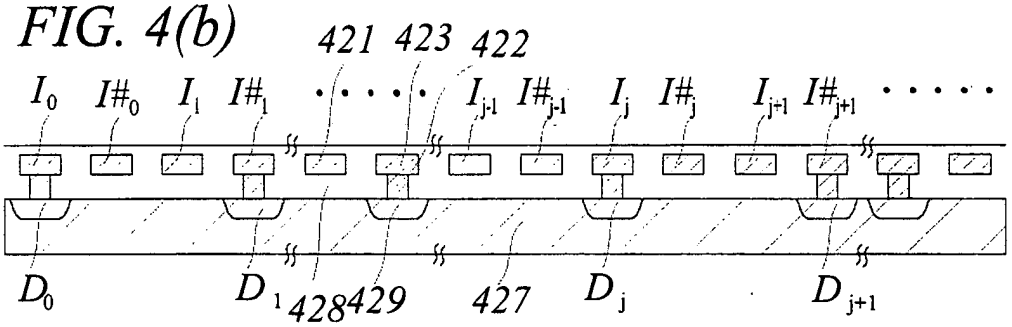
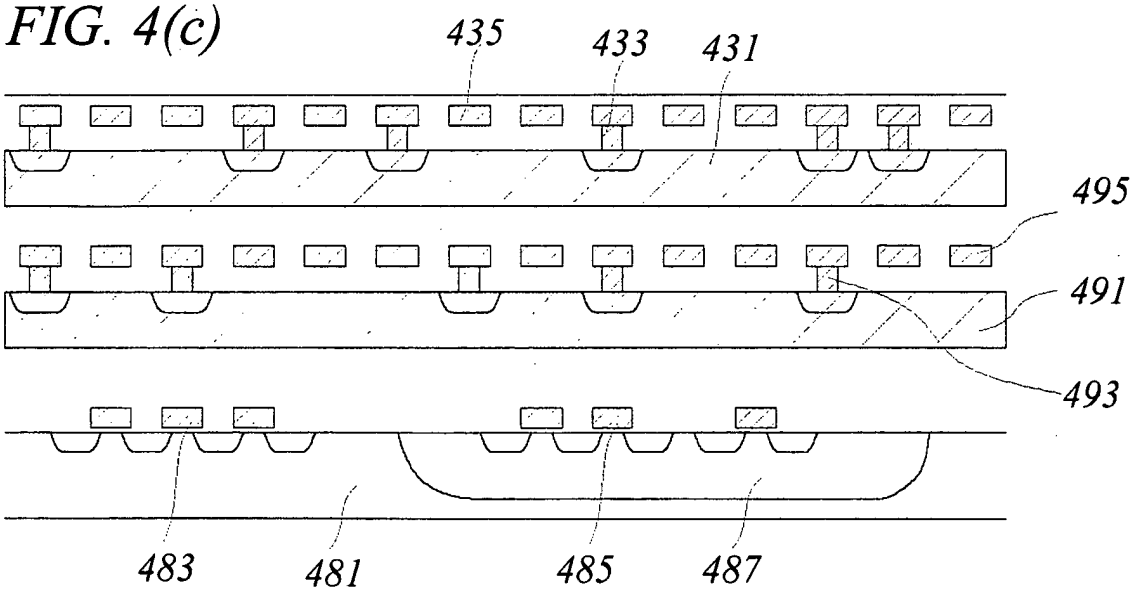
FIG. 4(c)